

74HC4094-Q100; 74HCT4094-Q100

8-stage shift-and-store bus register

Rev. 1 — 30 January 2013

Product data sheet

1. General description

The 74HC4094-Q100; 74HCT4094-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (D) and two serial outputs (QS1 and QS2) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the CP input. Data is available at QS1 on the LOW-to-HIGH transitions of the CP input to allow cascading when clock edges are fast. The same data is available at QS2 on the next HIGH-to-LOW transition of the CP input to allow cascading when clock edges are slow. The data in the shift register is transferred to the storage register when the STR input is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD7A
- Input levels:
 - ◆ For 74HC4094-Q100: CMOS level
 - ◆ For 74HCT4094-Q100: TTL level
- Low-power dissipation
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register



4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4094D-Q100 74HCT4094D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4094DB-Q100 74HCT4094DB-Q100	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4094PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

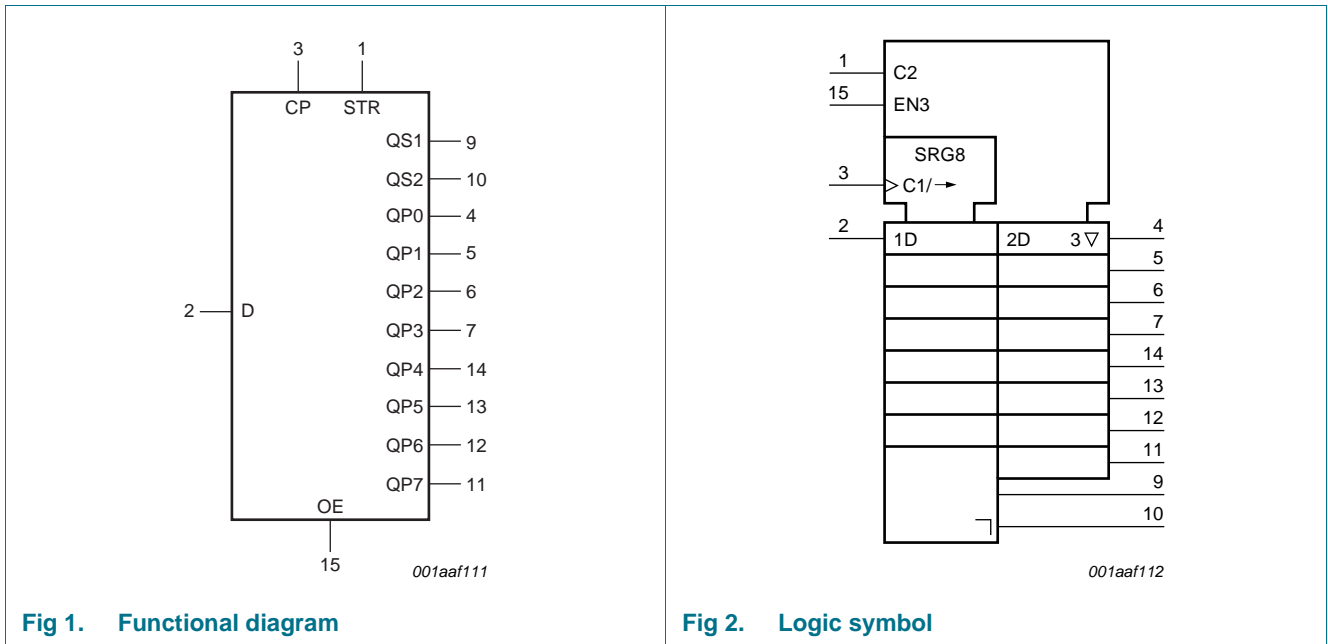


Fig 1. Functional diagram

Fig 2. Logic symbol

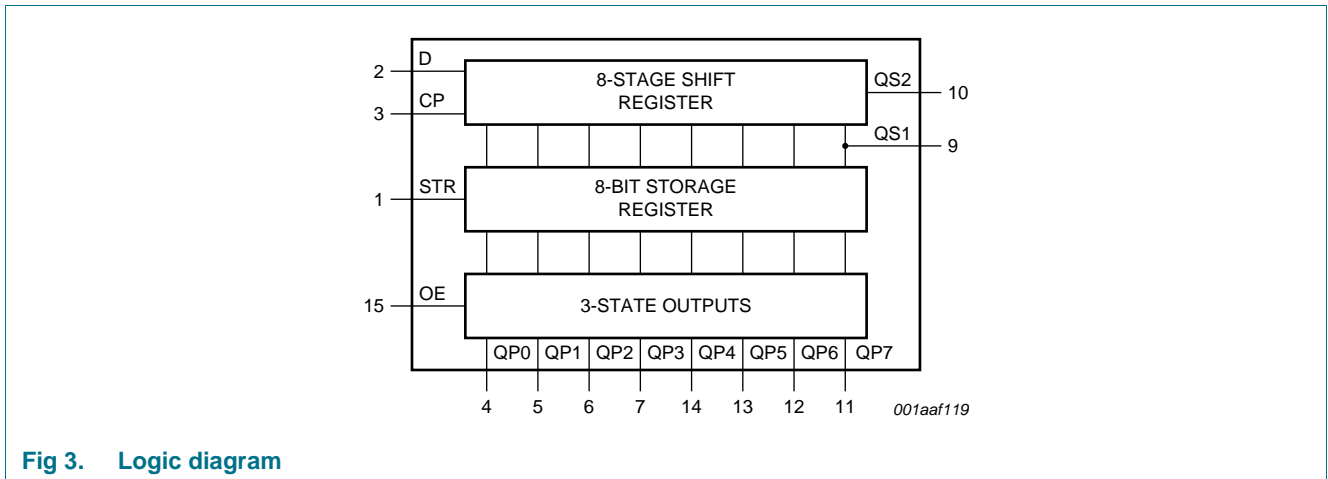


Fig 3. Logic diagram

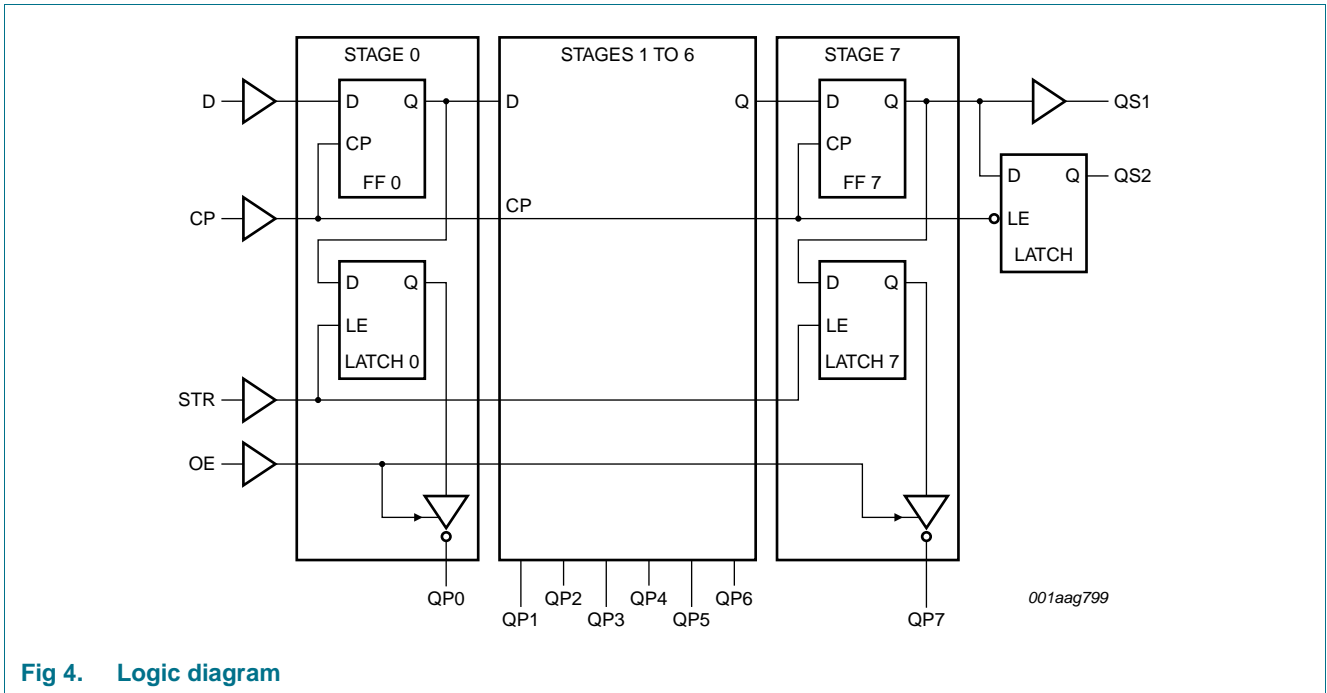


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

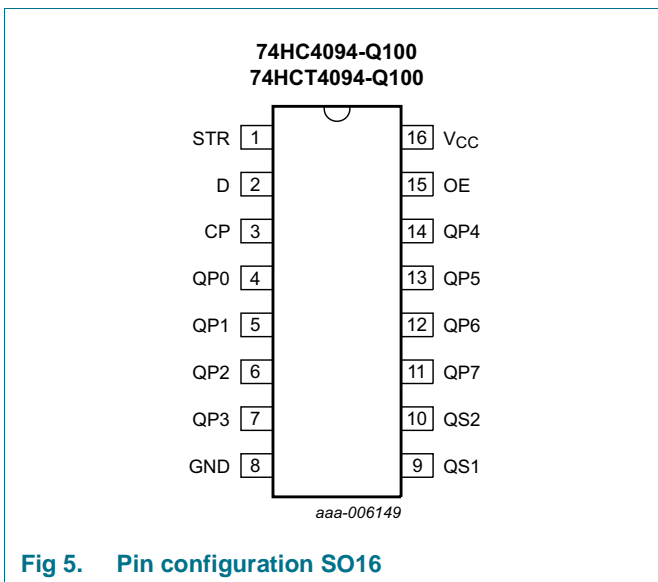


Fig 5. Pin configuration SO16

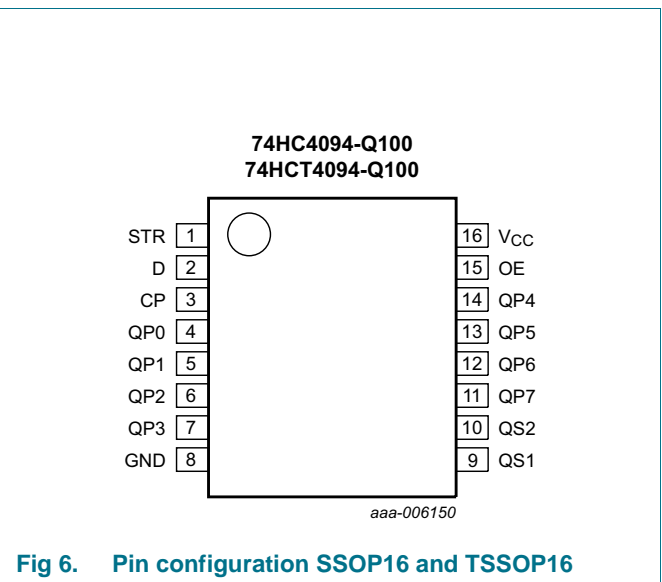


Fig 6. Pin configuration SSOP16 and TSSOP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output
V _{SS}	8	ground supply voltage
QS1, QS2	9, 10	serial output
OE	15	output enable input
V _{DD}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Inputs				Parallel outputs		Serial outputs	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn - 1	Q6S	NC
↑	H	H	H	H	QPn - 1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

- [1] At the positive clock edge, the information in the 7th register stage is transferred to the 8th register stage and the QSn outputs.
 H = HIGH voltage level; L = LOW voltage level; X = don't care;
 ↑ = positive-going transition; ↓ = negative-going transition;
 Z = HIGH-impedance OFF-state; NC = no change;
 Q6S = the data in register stage 6 before the LOW to HIGH clock transition;
 Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

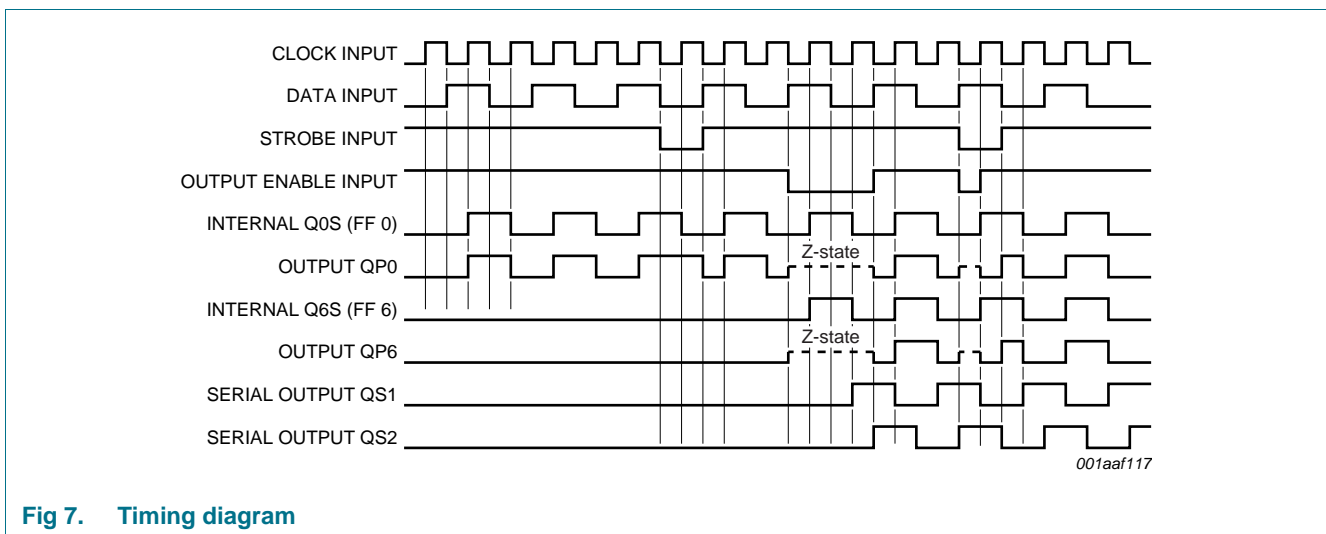


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation		[1] -	500	mW

[1] For SO16: P_{tot} derates linearly with 8 mW/K above 70 °C.

For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4094-Q100			74HCT4094-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit				
			Min	Typ	Max	Min	Max	Min	Max					
74HC4094-Q100														
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V				
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V				
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V				
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V				
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V				
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V				
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}												
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V				
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V				
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V				
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V				
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}												
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V				
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V				
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V				
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V				
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA				
		I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA		
				I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
				C _I	input capacitance		-	3.5	-				pF	
				74HCT4094-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V				
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V				
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V												
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V				
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V												
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V				
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V												
		I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V				
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V				

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$ A	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; STR input	-	100	360	-	450	-	490	µA
		per input pin; OE input	-	150	540	-	675	-	735	µA
		per input pin; CP input	-	150	540	-	675	-	735	µA
		per input pin; D input	-	40	144	-	180	-	196	µA
C_I	input capacitance		-	3.5	-					pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4094-Q100										
t_{pd}	propagation delay	CP to QS1; see Figure 8 ^[1]								
		$V_{CC} = 2.0$ V	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
		CP to QS2; see Figure 8 ^[1]								
		$V_{CC} = 2.0$ V	-	44	135	-	170	-	205	ns
		$V_{CC} = 4.5$ V	-	16	27	-	34	-	41	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	13	23	-	29	-	35	ns
		CP to QPn; see Figure 8 ^[1]								
		$V_{CC} = 2.0$ V	-	63	195	-	245	-	295	ns
		$V_{CC} = 4.5$ V	-	23	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	18	33	-	42	-	50	ns
		STR to QPn; see Figure 9 ^[1]								
$V_{CC} = 2.0$ V	-	58	180	-	225	-	270	ns		
$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	17	31	-	38	-	46	ns		
t_{en}	enable time	OE to QPn; see Figure 11 ^[2]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
t_{dis}	disable time	OE to QPn; see Figure 11 ^[3]								
		$V_{CC} = 2.0$ V	-	41	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	15	25	-	31	-	38	ns
		$V_{CC} = 6.0$ V	-	12	21	-	26	-	32	ns
t_t	transition time	QPn and QSn; see Figure 8 ^[4]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	CP HIGH or LOW; see Figure 8								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
		STR HIGH; see Figure 9								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
		t_{SU}	set-up time	D to CP; see Figure 10						
$V_{CC} = 2.0$ V	50			14	-	65	-	75	-	ns
$V_{CC} = 4.5$ V	10			5	-	13	-	15	-	ns
$V_{CC} = 6.0$ V	9			4	-	11	-	13	-	ns
CP to STR; see Figure 9										
$V_{CC} = 2.0$ V	100			28	-	125	-	150	-	ns
$V_{CC} = 4.5$ V	20			10	-	25	-	30	-	ns
$V_{CC} = 6.0$ V	17			8	-	21	-	26	-	ns
t_H	hold time			D to CP; see Figure 10						
		$V_{CC} = 2.0$ V	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5$ V	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0$ V	3	-2	-	3	-	3	-	ns
		CP to STR; see Figure 9								
		$V_{CC} = 2.0$ V	0	-14	-	0	-	0	-	ns
		$V_{CC} = 4.5$ V	0	-5	-	0	-	0	-	ns
		$V_{CC} = 6.0$ V	0	-4	-	0	-	0	-	ns
		f_{max}	maximum frequency	CP; see Figure 8						
$V_{CC} = 2.0$ V	6.0			28	-	4.8	-	4.0	-	MHz
$V_{CC} = 4.5$ V	30			87	-	24	-	20	-	MHz
$V_{CC} = 5$ V; $C_L = 15$ pF	-			95	-	-	-	-	-	MHz
$V_{CC} = 6.0$ V	35			103	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to V_{CC}	5	-	83	-	-	-	-	pF

Table 7. Dynamic characteristics ...continued

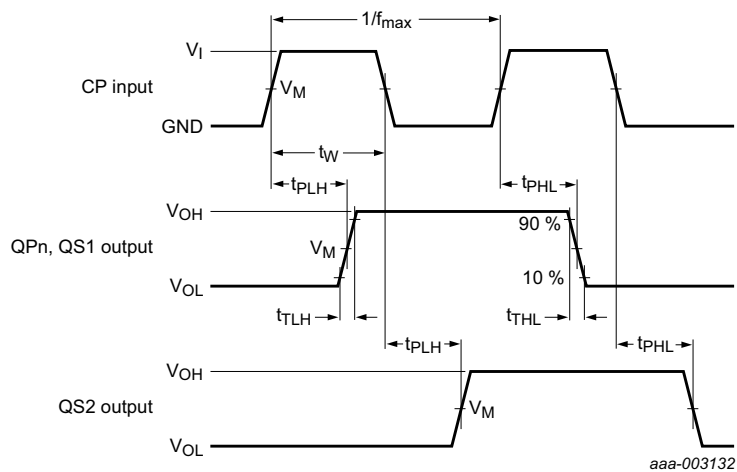
Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4094-Q100										
t_{pd}	propagation delay	CP to QS1; see Figure 8 [1]								
		$V_{CC} = 4.5$ V	-	23	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		CP to QS2; see Figure 8 [1]								
		$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
		CP to QPn; see Figure 8 [1]								
		$V_{CC} = 4.5$ V	-	25	43	-	54	-	65	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	21	-	-	-	-	-	ns
t_{en}	enable time	STR to QPn; see Figure 9 [1]								
		$V_{CC} = 4.5$ V	-	22	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
t_{dis}	disable time	OE to QPn; see Figure 11 [2]								
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
t_t	transition time	OE to QPn; see Figure 11 [3]								
		$V_{CC} = 4.5$ V	-	21	35	-	44	-	53	ns
t_t	transition time	QPn and QSn; see Figure 8 [4]								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
t_W	pulse width	CP HIGH or LOW; see Figure 8								
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
		STR HIGH; see Figure 9								
t_{su}	set-up time	Dn to CP; see Figure 10								
		$V_{CC} = 4.5$ V	10	4	-	13	-	15	-	ns
t_{su}	set-up time	CP to STR; see Figure 9								
		$V_{CC} = 4.5$ V	20	9	-	25	-	30	-	ns
t_h	hold time	Dn to CP; see Figure 10								
		$V_{CC} = 4.5$ V	4	0	-	4	-	4	-	ns
		CP to STR; see Figure 9								
t_h	hold time	$V_{CC} = 4.5$ V	0	-4	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Figure 8								
		$V_{CC} = 4.5$ V	30	80	-	24	-	20	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	86	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ [5]	-	92	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

- [2] t_{en} is the same as t_{PZH} and t_{PZL} .
- [3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [4] t_i is the same as t_{THL} and t_{TLH} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

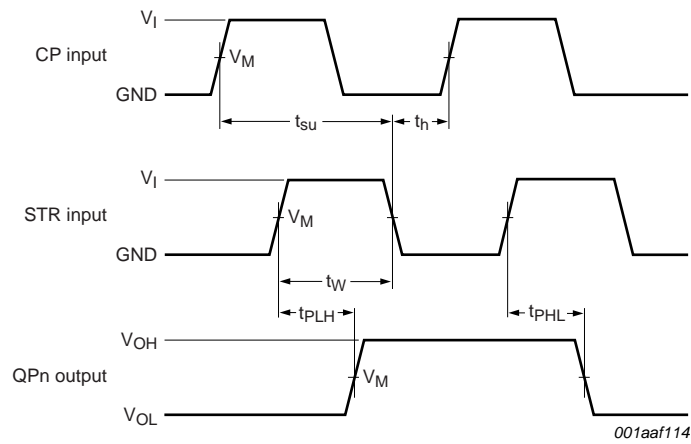
12. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

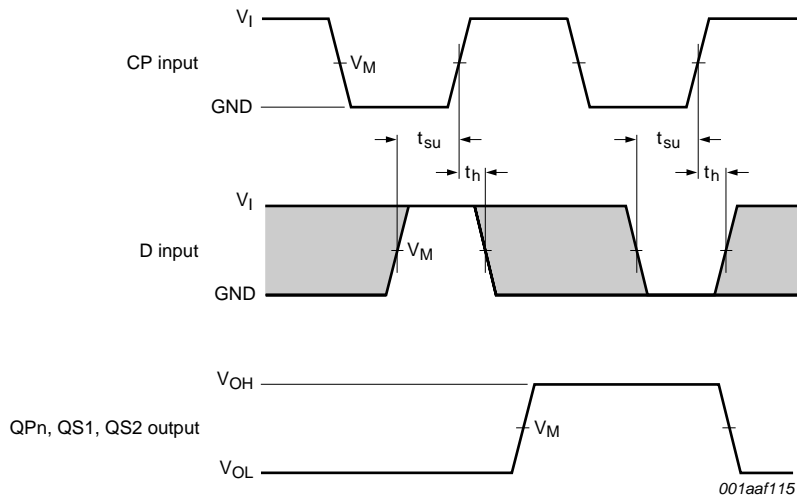
Fig 8. Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

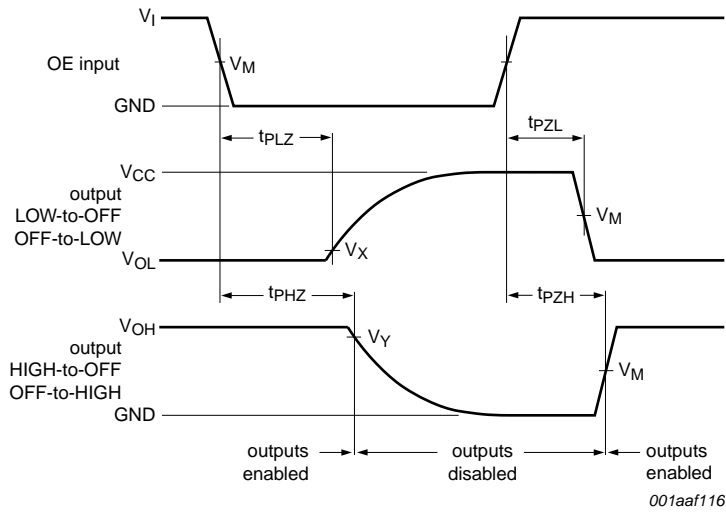
Fig 9. Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

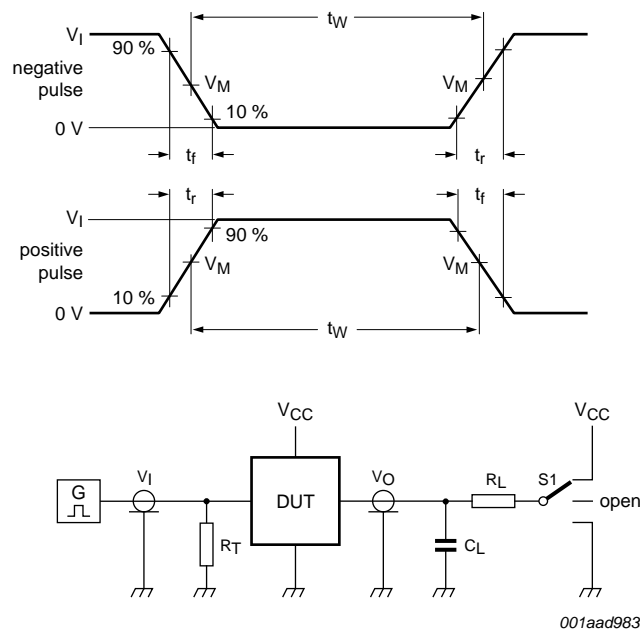


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 11. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC4094-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{OH}$	$0.9V_{OH}$
74HCT4094-Q100	1.3 V	1.3 V	$0.1V_{OH}$	$0.9V_{OH}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 12. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC4094-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT4094-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

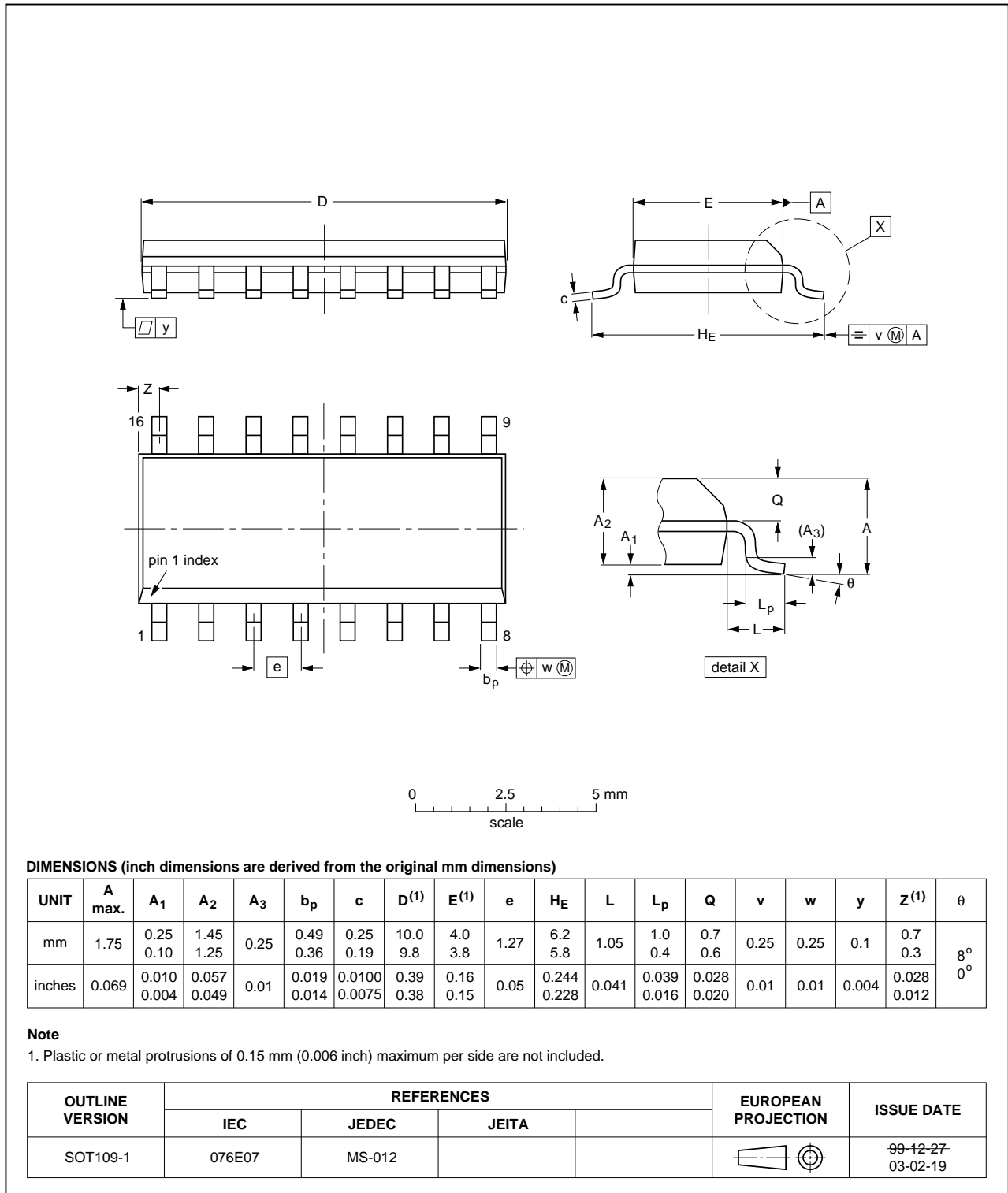


Fig 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

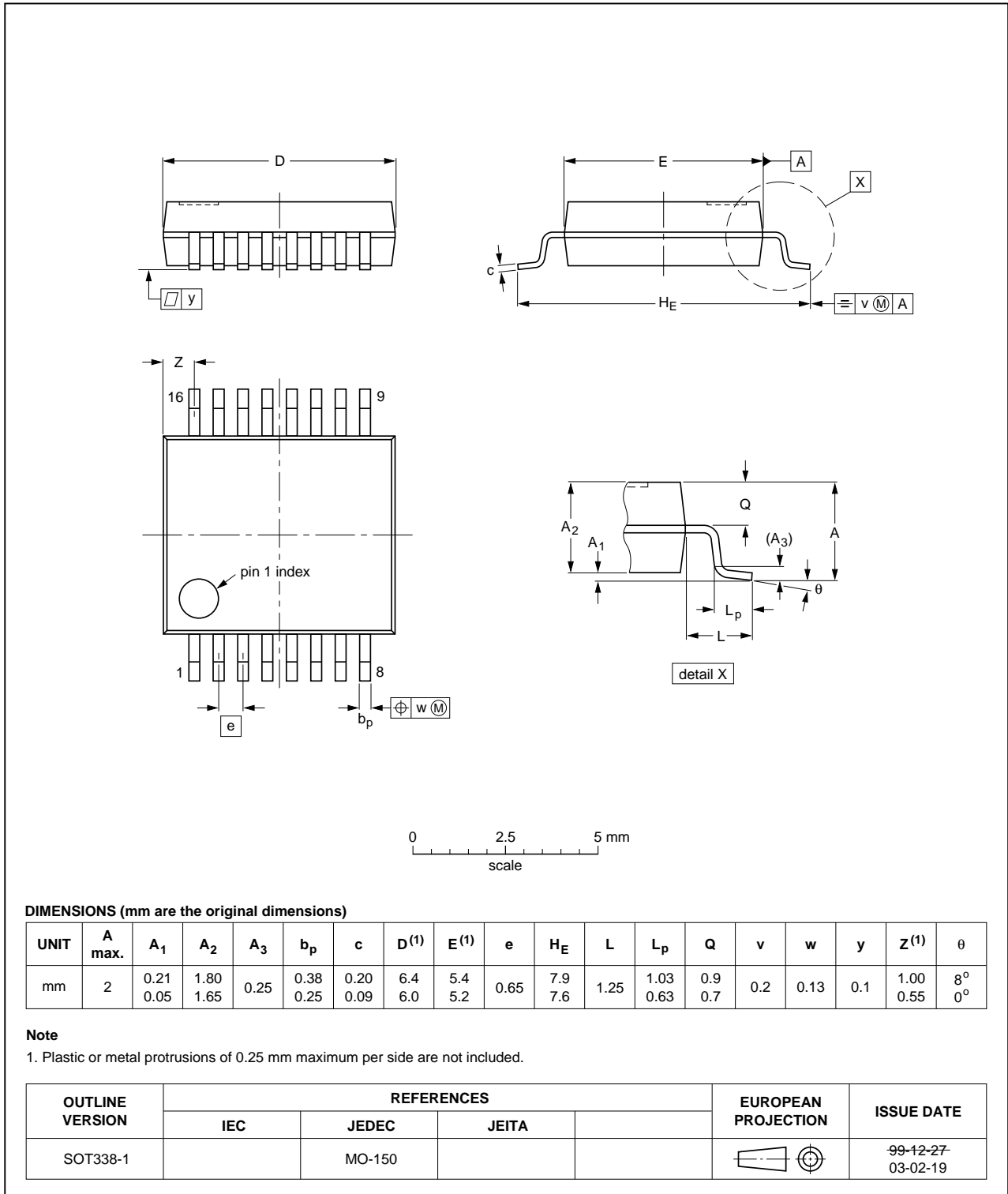


Fig 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

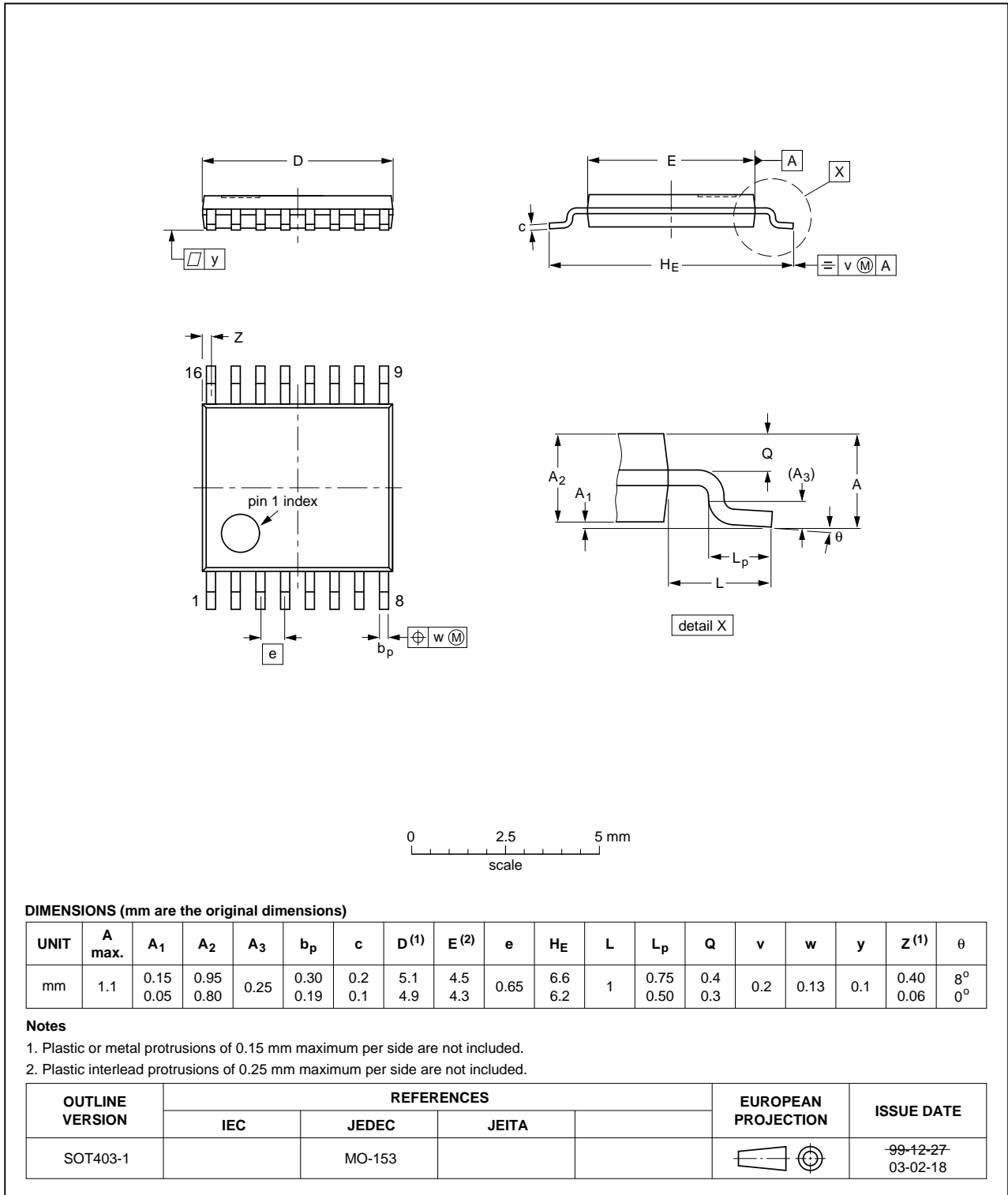


Fig 15. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4094_Q100 v.1	20130130	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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